# 6<sup>th</sup> International Symposium on Devices, Circuits and Systems

### **ISDCS 2023**

May 29-31, 2023 Hiroshima University, Higashi-Hiroshima, Japan



Co-Sponsored by:

**IEEE Hiroshima Section** 

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#### Foreword

It is the great pleasure of the entire Organizing Committee to announce the program of the 6<sup>th</sup> International Symposium on Devices, Circuits and Systems (ISDCS 2023) and to solicit your attendance. ISDCS 2023 will be held online with a home base in Hiroshima University, Higashi-Hiroshima, Japan, from May 29 to 31.

ISDCS focuses on the recent innovations of Devices, Circuits and Systems, highlighting the strong foundation in methodology and the integration of multidisciplinary approaches. Globally innovating scientists, researchers and engineers, who change the ways in which devices and circuits are understood, optimized, and leveraged in a variety of systems and applications, are cordially invited to attend and contribute to the discussions and scientific interactions at ISDCS concerning the presented latest research and development results.

This year, the ISDCS Program Committee received a total of fine submissions from 7 countries, of which 32 outstanding contributions would be included in the program ISDCS 2023. The Symposium has additionally 2 (two) eminent Keynotespeakersr and 9 (nine) renowned invited plenary speakers coming from Hiroshima University, IIEST Shibpur, NanoBridge Semiconductor, Inc., University of Michigan, IIT (ISM) Dhanbad, BITS Pilani, Hyderabad, DA-IICT Ahmedabad, Institute for Research in Fundamental Sciences, Teheran, Tokyo Institute of Technology, Shinshu Univ, IIT Gandhinagar and University of Bremen, Germany.

General Co-Chairs: Prof. Shinji Kaneko (Hiroshima University, Japan)
Prof. Hafizur Rahaman (IIEST, Shibpur, India)

#### Committee members

#### General Chair & Co-chair

- Shinji Kaneko, Hiroshima University, Japan
- Hafizur Rahaman, IIEST, Shibpur, India

#### **Program Chairs**

- Takahiro lizuka, Hiroshima University
- Chandan Giri, IIEST Shibpur

#### **Program Committee**

- Parthasarathi Chakrabarti, IIEST Shibpur, India
- Hafizur Rahaman, IIEST Shibpur, India.
- Koh Johguchi, Shinshu University, Japan
- Partha Roy Chaudhuri, IIT Kharagpur, India.
- Chika Tanaka, KIOXIA, Japan
- Bibhudatta Sahoo, IIT Kharagpur, India.
- Takao Yamamoto, DENSO Corp., Japan
- Partha Bhattacharyya, IIEST Shibpur, India.
- Tuhina Samanta, IIEST Shibpur, India.
- Hideki Murakami, National Institute of Technology, Kurume College
- Surajit K. Roy, IIEST Shibpur, India.
- Tsuyoshi Horikawa, Tokyo Institute of Technology, Japan
- Tapas Kumar Maiti, DA-IICT, India.
- Yutaka Sasaki, Hiroshima University, Japan
- Santanu Maity, IIEST Shibpur, India.
- Takeshi Kumaki, Ritsumeikan University, Japan
- Sandip Bhattacharya, SR University, India.
- Nillohit Mukherjee, IIEST Shibpur, India.
- Takeo Matsuki, AIST, Japan
- Parthasarathi Gupta, Global Foundries, India

#### **Publication Chair**

Subhajit Das, Hiroshima University

### Secretary

- Kaori Nishimoto, Hiroshima University
- Subhajit Das, Hiroshima University

#### **Advisory Board**

- Manabu Abe, Hiroshima University
- Parthasarathi Chakrabarti, IIEST Shibpur

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| Technical Program Table  |   |   |
|--|---|---|
| May 29   | May 30  | May 31  |
| (Monday)   | (Tuesday)   | (Wednesday)   |
| Session 1:   | Session 4:  | Session 7:  |
| Keynote Talks  Keynote Talk 1:  Prof. Shinji Kaneko, Hiroshima University, Japan  Keynote Talk 2:  Prof. Hafizur Rahaman, IIEST Shibpur, India  Session 2: | Devices, Circuits, Systems An Aggregated Subsystem Memory and Switching arrays, Interconnects Invited Talk: Dr. Nezam Rohbani, Institute for Research in Fundamental Sciences, Teheran Paper ID-(50, 30, 19, 15) Session 5: | Devices, Circuits, Systems An Aggregated Subsystem Memory and Switching arrays, Interconnects Invited Talk: Dr. Toshitsugu Sakamoto, NanoBridge Semiconductor, Inc., Japan Paper ID-(10, 8, 7) Session 8: |
| Optoelectronics and Nanotechnology<br>Invited Talk:<br>Dr. Sayan Kanungo, BITS Pilani, Hyderabad,<br>India   | Bridging Analog Digital Circuits, Algorithms, and Systems Invited Talk:   | Algorithms, Systems<br>Invited Talk:  |
| Paper ID- <mark>(38, 35, 20, 4</mark> ) Session 3:   | Dr. Mehdi Saligane, University of Michigan, USA  Paper ID-(48, 46, 37, 36)  Session 6:  | Dr. Manodipan Sahoo, IIT (ISM), Dhanbad<br>India<br>Paper ID-(16, 9, 6, 5)<br>Session 9:  |
| Device and Circuits— Sensing the World<br>in an Innovative Way<br>Invited Talk:<br>Dr. Neeraj Kaushal, IIT Gandhinagar, India                              | Intelligent Systems- Al Circuits and Systems<br>and Multimedia Signal Processing<br>Invited Talk:<br>Dr. Koh Joguchi, Shinshu University, Japan   | Intelligent Systems- Al Circuits and Systems and Multimedia Signal Processing Invited Talks:  Dr. Tapas Kumar Maiti, DA-IICT, India Prof. Rolf Drechsler, University of Bremer Germany                    |
| Paper ID- <mark>(47, 33, 32, 18)</mark>  | Paper ID-(51, 45, 41, 40, 39)   | Paper ID-(31, 21, 14, 3)  |

### **ISDCS 2023 Symposium Schedule**

### May 29, 2023

#### **Symposium Opening**

#### Session 1: Keynote Talks

 Town & Gown Initiative as a new strategy for establishing smart innovation ecosystem in university town in Japan.

Prof. Shinji Kaneko (Hiroshima University, Japan)

 Memristors Based In-memory Computing for Edge Computing Applications

Prof. Hafizur Rahaman (IIEST Shibpur, India)

#### Session 2: Devices -- Optoelectronics and Nanotechnology

### [Invited] Integration of the Two-dimensional Materials in Nano-scale MOSFET Design- Prospects and Challenges

Sayan Kanungo, BITS Pilani (Hyderabad), India

 Paper ID:38 - Influence of Kerr Nonlinearity on Dispersion-Shifted and Dispersion-Flattened Silica Fibers: An Accurate Finite Difference Analysis

Mitali Sahu and Partha Roy Chaudhuri (Indian Institute of Technology Kharagpur)

 Paper ID:35 - A New Approach of Designing All-fiber Band Rejection Filter based on Concatenated Multimode-Single mode-Multimode Fiber structure)

Protik Roy and Partha Roy Chaudhuri (Indian Institute of Technology Kharagpur)

 Paper ID:20 - Study of PbS Nanomaterial Sensitized ZnO based Solar Cell using SCAPS-1D Simulators Vishal Jha, Neha Kumari Shaw, Adrita Dasgupta, Debasmita Das, Somnath Dasgupta, and Abhigyan Ganguly (MAKAUT)

 Paper ID:4 - Effect of PV Soiling on Day-ahead Scheduling of a Grid Integrated Microgrid
 Saheli Sengupta, Chandan Kumar Chanda, Hiranmay Saha and Samarjit Sengupta (SAMGESS, IIEST, Shibpur)

# Session 3: Device and Circuits— Sensing the World in an Innovative Way

### [Invited] Advancing High Voltage MOS Transistor Compact Models Through Physical Augmentation: Techniques and Applications

Dr. Neeraj Kaushal, Indian Institute of Technology Gandhinagar, India

- Paper ID:47 Design of an Optimized Micro-heater using Soft-Computing Tools for Low Temperature Gas Sensing Application Gour Gopal Jana (Greater Kolkata College of Engineering and Management), Jyotirmoy Nandy (Home Department, Govt. of West Bengal, Kolkata), Subhashis Roy (Techno India University, Kolkata) and Bijoy Kantha (Netaji Subhash Engineering College, Kolkata)
- Paper ID:33 Experimental Demonstration of All-Fiber Electric Field Sensing Device Isha Sharma and Partha Roy Chaudhuri (Indian Institute of Technology Kharagpur).
- Paper ID:32 Selective Review on Dielectric modulated Tunnel FET based Biosensor
   Vishal Jha, Debasmita Manna, and Dr. Sangeeta Jana Mukhopadhyay (Dr. Sudhir Chandra Sur Institute of Technology and Sports Complex)
- Paper ID:18 Photodiode and Analog-Front-End Circuit Design for Wearable Vital Sensing System with Fiber-Bragg-Grating Sensor Kaede Kano and Koh Johguchi (Shinshu University).

### May 30, 2023

# Session 4: Devices, Circuits, Systems --- An Aggregated Subsystem --- Memory and Switching arrays, Interconnects

#### [Invited] PF-DRAM: A Precharge-Free DRAM Structure

Dr. Nezam Rohbani, Institute for Research in Fundamental Sciences. Teheran

- Paper ID:50 Design of CMOS Memristor Emulator and Logic Gates For Neuromorphic Circuits
  - K.Shabd Swaroop and Gufran Ahmad (Department of Electrical Engineering, DAYALBAGH EDUCATIONAL INSTITUTE (DEEMED UNIVERSITY), AGRA, INDIA)
- Paper ID:30 Electro-thermal modeling of Multilayer Graphene Nanoribbon (MLGNR) Interconnect considering Energy-per-Layer Screening
  - Santasri Giri Tunga (Indian Institute of Engineering Science and Technology), Subhajit Das (Indian Institute of Engineering Science and Technology), Sandip Bhattacharya (SR University) and Hafizur Rahaman (Indian Institute of Engineering Science and Technology)
- Paper ID:19 Generation of Broadband Supercontinuum by a Sodesigned Silicon on Insulator (SOI) Rectangular Buried Waveguides Tiyas Das (IIEST Shibpur) and Mousumi Basu (IIEST Shibpur Physics department).
- Paper ID:15 Switching Activity Reduction in Graphene PN Junction Circuits using Circuit Re-structurings
  - Subrata Das (Dept. of CSE, Sister Nivedita University), Arighna Deb (School of Electronics Engineering, KIIT DU) and Petr Fiser (Faculty of Information Technology, Czech Technical University).

# Session 5: Bridging Analog Digital Circuits, Algorithms, and Systems

### [Invited] OpenFASOC: An Open platform towards analog and mixedsignal analog automation and democratizing chip design

Dr. Mehdi Saligane, University of Michigan, USA

- Paper ID:48 Implementation of Area Efficient Adders for Inexact Computing
  - Rounak Roy, Sudip Ghosh, and Hafizur Rahaman (Indian Institute of Engineering Science and Technology, Shibpur)
- Paper ID:46 Target Voltage Control Approach for Active Distribution System Based on PV Active and Reactive Powers Nodal Prices Ryuta Kubo, Naoto Yorino, Yoshifumi Zoka, Yutaka Sasaki, Satoshi Taoka (Hiroshima University) and Ahmed Bedawy (Hiroshima University, South Valley University)
- Paper ID:37 Design of High Gain Low-Noise Amplifier at X-Band Frequency
   Shrabanti Das, Posiba Mostafa, and Sayan Chatterjee (JADAVPUR UNIVERSITY)
- Paper ID:36 A Multiphase Low Phase-Noise DCO based on Self-Timed Ring Oscillator
   Posiba Mostafa and Sayan Chatterjee (Jadavpur University)

# Session 6: Intelligent Systems- Al Circuits and Systems and Multimedia Signal Processing

### [Invited] Smart Sensing Circuit Design in IoT Era

Dr. Koh Joguchi, Shinshu University, Japan

Paper ID:51 - Security Attacks on Social Networking: A Review
 Priti Halder and Malay Kule (Indian Institute of Engineering Science and Technology, Shibpur)

- Paper ID:45 Deep Learning Based Real Time Face Recognition for University Attendance System
   Mansi Singhal and Gufran Ahmad (Department of Electrical Engineering, DAYALBAGH EDUCATIONAL INSTITUTE (DEEMED UNIVERSITY), AGRA, INDIA)
- Paper ID:41 Fighting Deepfakes by Detecting DCT Frequency Anomalies
   Arnab Kumar Das, Soumik Mukhopadhyay, Arijit Dalui, Ritaban Bhattacharya and Ruchira Naskar (Indian Institute of Engineering Science and Technology, Shibpur)
- Paper ID:40 Emotion Recognition from EEG Signals Based on Optimization Of Mutual Information Snigdha Madhab Ghosh, Sharba Bandyopadhyay (Indian Institute of Technology, kharagpur), and Debjani Mitra (Indian Institute of Technology (ISM), Dhanbad)
- Paper ID:39 Neural Network Architectures for Integrated Circuits
   Khyati Nagrani, and Tapas Kumar Maiti (Dhirubhai Ambani Institute of
   Information and Communication Technology).

### May 31, 2023

# Session 7: Devices, Circuits, Systems --- An Aggregated Subsystem --- Memory and Switching arrays, Interconnects

[Invited] Low power programmable logic using NanoBridge technology Dr. Toshitsugu Sakamoto, Co-founder, NanoBridge Semiconductor, Inc. Japan.

- Paper ID:10 Negative Impact of Approximated Signed Addition on Power Reduction
  - Hiroyuki Hama, Tomoaki Ukezono, and Toshinori Sato (Fukuoka University).
- Paper ID:8 Dynamic Frequency Control of a Low Inertia Microgrid using Virtual Synchronous Generator Supriya Sharma, Samarjit Sengupta, Mrinmoy Chattopadhyay, and Hiranmay Saha (School of Advanced Materials Green Energy and Sensor Systems, IIEST, Shibpur)
- Paper ID:7 Simulation-Based Switching Performance Self-Heating Effect on SiC-based Power-Electronic Circuits Subhajit Das (Hiroshima University) and Takahiro lizuka (Hiroshima University).

# Session 8: Bridging Analog and Digital Circuits, Algorithms, Systems

[Invited] Design of low-power and high-performance SRAM using Electrostatically doped TMD TFET for the 10 nm node

Dr. Manodipan Sahoo, IIT (ISM) Dhanbad, India

- Paper ID:16 Temperature Sensor Circuit for a Wearable Perspiration Monitoring System
   Yuichiro Ichimura, Kenta Goto, and Koh Johguchi (Shinshu University).
- Paper ID:9 An Intelligent Grid integrated BESS Solar PV System to Supply Critical Loads under Grid Outage Condition

Mrinmoy Chattopadhyay, Supriya Sharma, Hiranmay Samanta, Samarjit Sengupta, and Hiranmay Saha (School of Advance Materials, Green Energy and Sensor System, IIEST Shibpur).

Paper ID:6 - Frequency resilient operation strategy of an autonomous microgrid

Sourish Basu, Chayan Bandyopadhyay, Samarjit Sengupta, and Hiranmay Saha (SAMGESS, IIEST, Shibpur)

 Paper ID:5 - An intelligent technique to minimize the loss of load under grid outage condition in a grid connected microgrid Chayan Bandyopadhyay, Sourish Basu, Hiranmay Samanta, Samarjit Sengupta, and Hiranmay Saha (SAMGESS, IIEST, Shibpur)

# Session 9: Intelligent Systems- Al Circuits and Systems and Multimedia Signal Processing

### [Invited] Robot Movement Visualization Based on Component-Oriented Simulation

Dr. Tapas Kumar Maiti, DA-IICT, Ahmedabad, India

### [Invited] Towards Polynomial Formal Verification of Al-Generated Arithmetic Circuits

Prof. Rolf Drechsler, University of Bremen, Germany

 Paper ID:31 - Hybrid Genetic Algorithm Random Forest algorithm (HGARF) for improving the missing value imputation in Hepatitis medical dataset

Pijush Dutta (Greater Kolkata College of Engineering and Management), Shobhandeb Paul (Guru Nanak Institute of Technology), Arindam Sadhu (Greater Kolkata College of Engineering and Management) and Gour Gopal Jana (Greater Kolkata College of Engineering and Management)

 Paper ID:21 - A comprehensive review on ReRAM-based accelerators for deep learning

Pooja Joshi and Hafizur Rahaman (Indian Institute of Engineering, Science and Technology (IIEST), Shibpur, India)

 Paper ID:14 - Resource-efficient VLSI Architecture of Softmax Activation Function for Real-time Inference in Deep Learning Applications

Akash Ther, Binit Kumar Pandit (Indian Institute of Engineering Science and Technology, Shibpur Howrah (W.B.)), Anirban Ganguly (Bharat Institute of Engineering and Technology, Hyderabad (T.S.)), Anirban Chakraborty (University of Engineering and Management, Kolkata (W.B.)) and Ayan Banerjee (Indian Institute of Engineering Science and Technology, Shibpur Howrah (W.B.))

 Paper ID:3 - Intelligent Transportation of Heterogeneous droplets in DMFB: A Preferential Deviation Based Technique Pranab Roy (J. K Laxmipat University, Jaipur), Sarit Chakraborty (Govt. College

of Engineering and Leather Technology, Kolkata, India), Rupam Bhattacharya (I. E. M, Kolkata), Priyotosh Jana (Haldia Institute of Technology, WB), Paramita Dey (Government College of Engineering and Ceramic Technology, Kolkata) and Susanta Chakraborty (IIEST-Shibpur)



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